Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : BOM Changes (LF plating and DA) on VIPER products (TFME subcon as assy plant).

PCN Reference : AMS/22/13129

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

VIPER26LN	VIPER17HN	VIPER26HN
VIPER06XN	VIPER27HN	VIPER16LN
VIPER06LN	VIPER17LN	VIPER27LN
VIPER06HN	VIPER16HN	VIPER28HN
VIPER28LN		

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Reliability Report
RR001221CO6410

General Information	
Product Line	*MT13 (UA68+VZ81)*
Product Description	*Off-line Converter*
Package	*DIP7*
Silicon Technology	*BCD6 (UA68)* *Supermesh (VZ81)*

Traceability	
Diffusion Plant	*Catania* *Ang Mo Kio (Singapore)*
Assembly Plant	*TFME*

Reliability Assessment	
Pass	☒
Fail	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Content description	Date	Author	Function
1.0	Initial Revision	05-Mar-21	P. Teruzzi/G. Capodici	Reliability Engineer

APPROVED BY:

Function	Location	Name
Division Reliability Manager	Italy	A. Paratore
Division Quality Manager	Italy	A. Platini

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

MT13 is an already qualified device. This report contains the reliability evaluation of MT13 device diffused in Catania/Ang Mo Kio and assembled in Dip7 in TFME, in the overall plan of 8200T Glue and DIP7LM(S-Ag) with Cu Ring lead frame qualification including also other test vehicle.

1.2 Reliability Strategy

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification and are listed in below Test Plan. For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.3 Conclusion

All reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing.

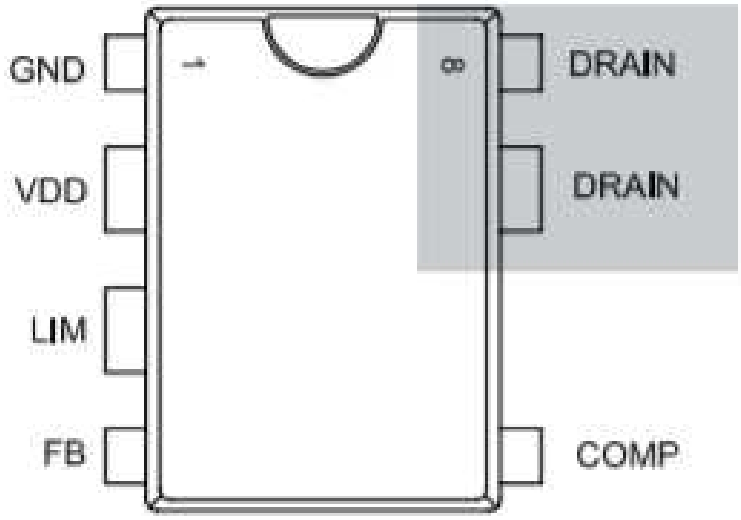
Based on the overall results obtained, MT13 device diffused in Catania/Ang Mo Kio and assembled in Dip7 in TFME, has positively passed reliability evaluation.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

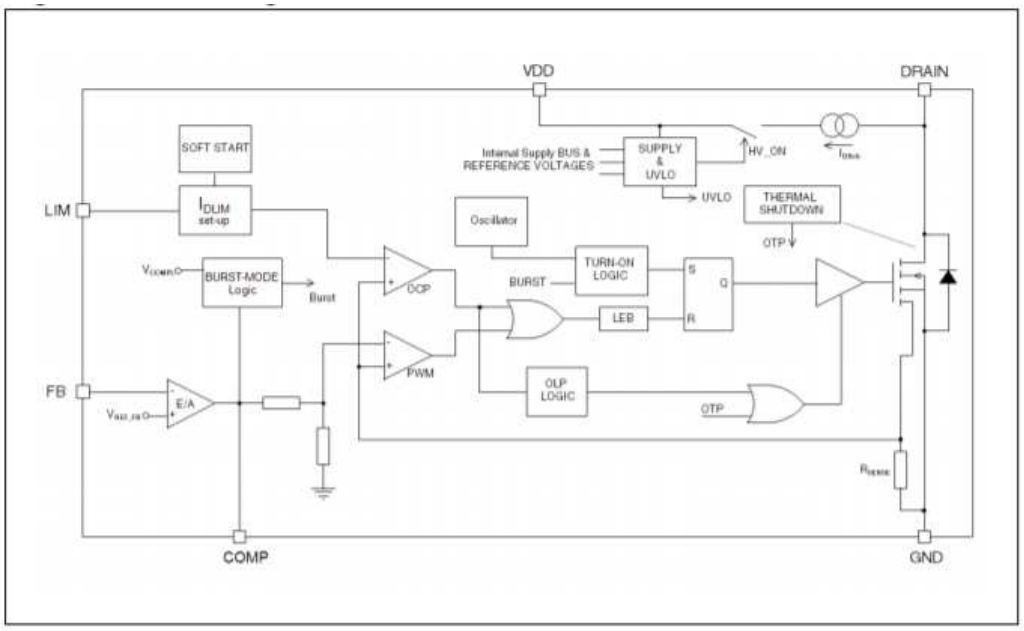
2.1 Generalities

The device is an off-line converter with an 800 V avalanche ruggedness power section, a PWM controller, user defined overcurrent limit, protection against feedback network disconnection, hysteretic thermal protection, soft start up and safe auto restart after any fault condition.

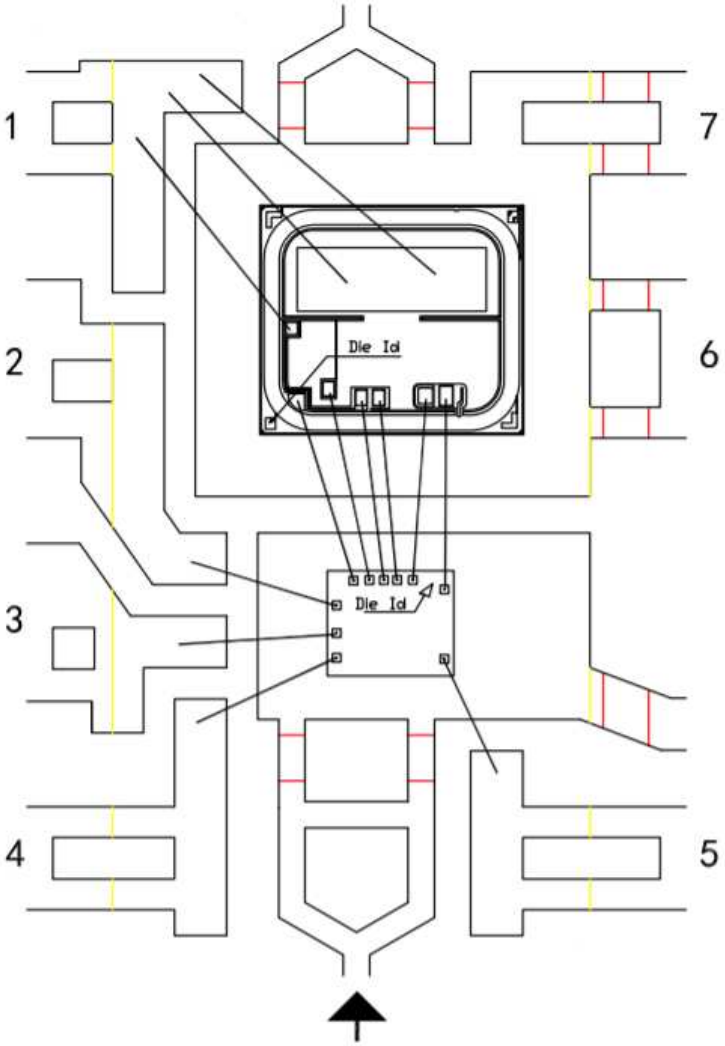
2.2 Pin connection



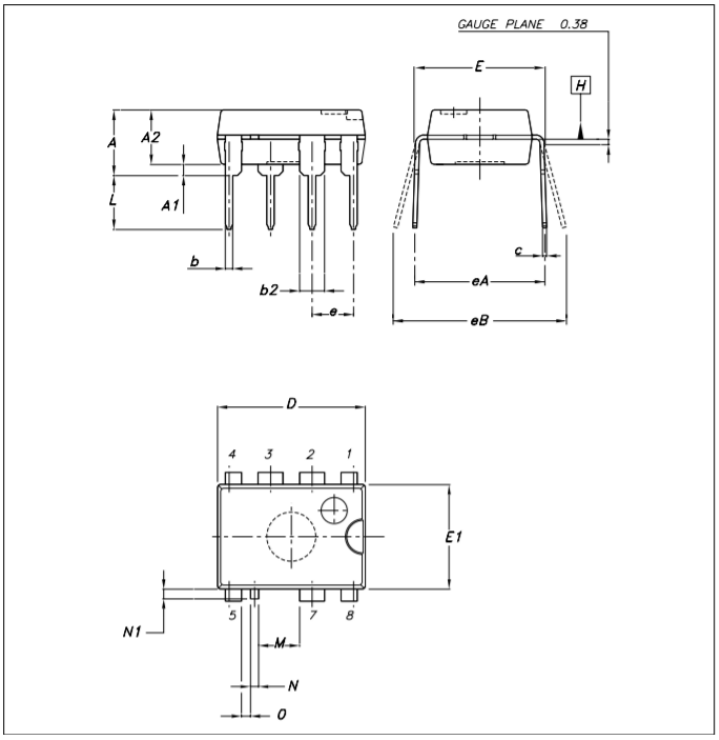
2.3 Block diagram



2.4 Bonding diagram



2.5 Package Outline / Mechanical data



Dim.	mm		
	Typ	Min	Max
A			5.33
A1		0.38	
A2	3.30	2.92	4.95
b	0.46	0.36	0.56
b2	1.52	1.14	1.78
c	0.25	0.20	0.36
D	9.27	9.02	10.16
E	7.87	7.62	8.26
E1	6.35	6.10	7.11
e	2.54		
eA	7.62		
eB			10.92
L	3.30	2.92	3.81
M	2.508		
N	0.50	0.40	0.60
N1			0.60
O	0.548		

2.6 Traceability

2.6.1 Wafer fab information

Table 1

Wafer fab information	
UA68	
Wafer fab name / location	CATANIA
Wafer diameter (inches)	8
Die thickness (µm)	375
Silicon process technology	BCD6
Die finishing front side (passivation)	TEOS/SiN/Polymide
Die finishing back side	RAW SILICON SINGLE GRIND
Die area (X,Y) (µm)	1320,1112
Metal levels	3
Bond Pad Material	Ti/AlCu/TiNARC

Table 2

Wafer fab information	
VZ81	
Wafer fab name / location	Ang Mo Kio – Singapore
Wafer diameter (inches)	6
Die thickness (µm)	280
Silicon process technology	Supermesh
Die finishing front side (passivation)	SiN (nitride)
Die finishing back side	Ti/Ni/Au
Die area (X,Y) (µm)	2650,2320
Metal levels	1
Bond Pad Material	AlSi

2.6.2 Assembly information

Table 3

Assembly Information	
DIP7	
Assembly plant name	*TFME*
Lead frame finishing (material)	*DIP7LM Cu Ring*
Die attach material	*ABLEBOND 8200T*
Wire bonding material/diameter	*D1.0 AU WIRE*
Molding compound material	*EMG-400-1F (HHCK)*

2.6.3 Reliability information

Table 4

Reliability Information	
Reliability laboratory name / location	Agrate-Cornaredo / Italy (lot 1,2,3,7) Muar / Malaysia (lot 4,5,6)

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 5

Lot #	Diffusion Lot	Die Revision (Cut)	Raw Line	Package	Note
1	V584258M	BE6	FEJG*MV61BE6	DIP7	Equivalent Test vehicle
2	V5840WY9	BG6	RFJG*MV34BG6	DIP7	Equivalent Test vehicle
3	V5819UU6	AEX	FU(E*MT19AEX	SDIP10	Equivalent Test vehicle
4	V5009H09	AC6	1UJG*MT13AC6	DIP7	
5	V50121WF	BE6	1UJG*MV61BE6	DIP7	Equivalent Test vehicle
6	V5017W75	BG6	1UJG*MV34BG6	DIP7	Equivalent Test vehicle
7	KYA938	AA5	A5(E*MT13AA5	DIP7	Equivalent Test vehicle

3.2 Test plan and results summary

Table 6 – ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	VCC=23V TJ=150°C Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	45	135	Lot 1: 0 / 45 Lot 2: 0 / 45 Lot 3: 0 / 45	
HTRB	JESD22 A108	VDRAIN=640V VCC=23V TJ=150°C Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	45	135	Lot 1: 0 / 45 Lot 2: 0 / 45 Lot 3: 0 / 45	

Note: Test method revision reference is the one active at the date of reliability trial execution.

Table 7 – ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
THB	JESD22 A101	VDRAIN=100V VCC=23V Ta=85°C, 85%RH, Duration= 1000hrs ☐ After PC ☒ Testing at Room	2 1	40 25	80 25	Lot 1: 0 / 40 Lot 2: 0 / 40 Lot 3: 0 / 25	
TC	JESD22-A104	Ta= Duration= 500cy ☐ After PC ☒ Testing at Room	3 1	25 77	75 77	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25 Lot 4: 0 / 77 Lot 5: 0 / 77 Lot 6: 0 / 77	
AC	JESD22 A102	P=2.08atm Ta=121°C, Duration = 96hrs ☐ After PC ☒ Testing at Room	3	25	75	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25	
HTSL	JESD22 A103	Ta= 150ºC Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	25	75	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25	

Note: Test method revision reference is the one active at the date of reliability trial execution.

Table 8 – ELECTRICAL VERIFICATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results Fail/S.S.	Comments: (N/A =Not Applicable)
CDM	ANSI/ESD STM 5.3.1-2009	CDM=+/-1500V ☒ Testing at Room	1	3	3	Lot 7 :0 / 3	
MM	EIA/JESD22-A115	MM=+/-200V ☒ Testing at Room	1	3	3	Lot 7 :0 / 3	
HBM	ANSI/ESDA/JEDEC JS001-2014	HBM=+/-4000V ☒ Testing at Room	1	3	3	Lot 7 :0 / 3	
LU	JESD78	Current Injection Class II - Level B (+/- 100mA) Overvoltage Class II - Level B (1,5 x Vmax) ☐ Testing at Room	1	6	6	Lot 7 :0 / 6	

Note: Test method revision reference is the one active at the date of reliability trial execution.

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
AEC-Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits in automotive applications
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
DMS 0061692	Reliability Tests and Criteria for Product Qualification

5 GLOSSARY

List update based on applicable items.

AC	Autoclave
ACBV	AC Blocking Voltage
ASER	Accelerated Soft Error Rate
AST	Adhesion Shear Test
BI	Burn-In
BT3P	Board 3 points Bending Test
BT4P	Board 4 points Bending Test
CA	Constant Acceleration
CDM	Electrostatic Discharge – Charged Device Model
ConA	Construction Analysis
CVS	Constant Voltage Stress
DBT	Dead Bug Test
DPA	Destructive Physical Analysis
DROP	Package drop
DS	Die Shear
DToB	Drop Test on Board
EDR	NVM Program/Erase Endurance & Data Retention Stress Test
ELFR	Early Life Failure Rate
EMC	Electromagnetic Compatibility
EOS	Electrical Overstress characterization
ESeq	Environmental sequence
EV	External Visual
GFF	
GFL	Gross/Fine Leak
GL	Electro-thermally Induced Gate Leakage
GStress	Gate Stress
GUN	Electrostatic Discharge – System Level Test
H3TRB	High Humidity High Temperature Reverse Bias
HAST	Biased HAST (Highly Accelerated Stress Test)
HBM	Electrostatic Discharge – Human Body Model
HER	Hermeticity
HMM	Electrostatic Discharge – Human Metal Model
HTFB	High Temperature Forward Bias
HTGB	High Temperature Gate Bias
HTHHB	High Temperature High Humidity Bias
HTOL	High Temperature Operating Life
HTRB	High Temperature Reverse Bias.
HTSL	High Temperature Storage Life
IOL	Intermittent Operating Life
IWV	Internal Water Vapor
LF	Lead Free
LI	Lead Integrity
LT	Lid Torque
LTOL	Low Temperature Operating Life
LTSL	Low Temperature Storage Life
LU	Latch-Up
MM	Electrostatic Discharge – Machine model

MR	Multiple Reflow
MS	Mechanical Shock
MSeq	Mechanical sequence
MSL	Moisture Sensitivity Level
NVM	Non Volatile Memory
PC	Preconditioning
PD	Physical Dimensions
PTC	Power Temperature Cycling
RS	Repetitive Surge Test
TSH	Resistance to Solder Heat
RTSER	Real-Time Soft Error Rate
SAM	Scanning Acoustic Microscopy
SBP	Solder Ball Pull
SBS	Solder Ball Shear
SC	Short Circuit Characterization
SCCSS	Smartcard – Constant Supply Stress
SCMCMS	Smartcard – MasterCard Mechanical Stress
SCMF	Smartcard – Magnetic Field Stress
SCPOOS	Smartcard – Power Off/On Stress
SCRFC	Smartcard – RF On/Off Cyclic Stress
SCRFS	Smartcard – RF On Static Stress
ScrT	Screw Test
SCSA	Smartcard – Salt Atmosphere
SCUV	Smartcard – UV Test
SCXRAY	Smartcard – XRAY Test
SD	Solderability
SSOP	Steady State Operational
SToB	Shock Test on Board
TC	Temperature Cycling
TCDT	Temperature Cycling Delamination Test
TCHT	Temperature Cycling Hot Test
TCoB	Temperature Cycling on Board
THB	Temperature Humidity Bias
THS	Temperature Humidity Storage
TLP	Electrostatic Discharge – Transmission Line Pulse
TS	Thermal Shocks
TStr	Terminal Strength
Tumb	Tumbler Test
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
VToB	Vibration Test on Board
VFV	Variable Frequency Vibration
WAT	Tin (Sn) Whisker Acceptance Testing
WBI	Wire Bond Integrity
WBP	Wire Bond Pull
WBS	Wire Bond Shear
WBSt	Wire Bond Strength
XRAY	X ray inspection

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Reliability Report
RR001321CO6410

General Information	
Product Line	*MV34 (UL39 + VZ8Q)*
Product Description	*Off-line Converter*
Package	*DIP7*
Silicon Technology	*BCD6 (UL39)* *Supermesh (VZ8Q)*

Traceability	
Diffusion Plant	*Catania* *Ang Mo Kio (Singapore)*
Assembly Plant	*TFME*

Reliability Assessment	
Pass	☒
Fail	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Content description	Date	Author	Function
1.0	Initial Revision	05-Mar-21	P. Teruzzi/G. Capodici	Reliability Engineer

APPROVED BY:

Function	Location	Name
Division Reliability Manager	Italy	A. Paratore
Division Quality Manager	Italy	A. Platini

Table of Contents

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

MV34 is an already qualified device. This report contains the reliability evaluation of MV34 device diffused in Catania/Ang Mo Kio and assembled in DIP7 in TFME, in the overall plan of 8200T glue and DIP7LM(S-Ag) with Cu Ring lead frame qualification including also other test vehicle.

1.2 Reliability Strategy

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification and are listed in below Test Plan. For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.3 Conclusion

All reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing.

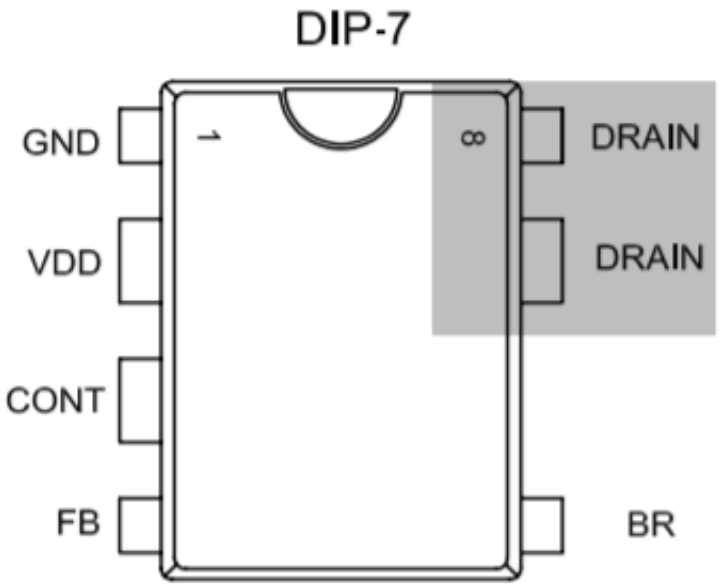
Based on the overall results obtained, MV34 device diffused in Catania/Ang Mo Kio and assembled in Dip7 in TFME, has positively passed reliability evaluation.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

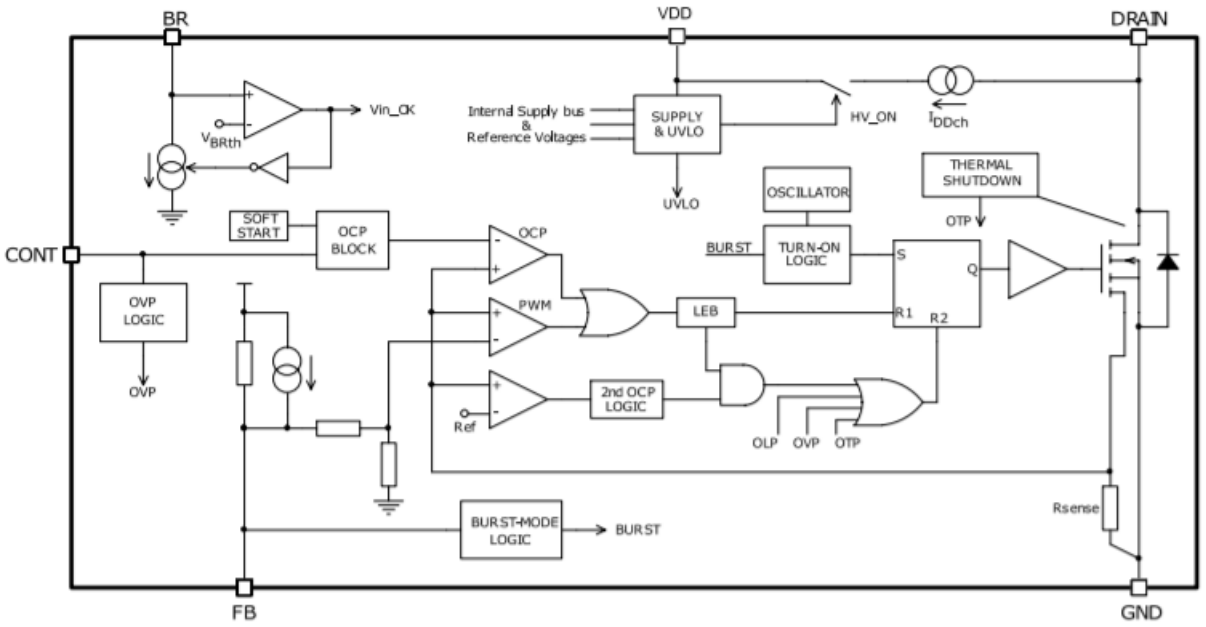
2.1 Generalities

The device is an off-line converter with an 800 V rugged power section, a PWM control, two levels of overcurrent protection, overvoltage and overload protections, hysteresis thermal protection, soft-start and safe auto-restart after any fault condition removal.

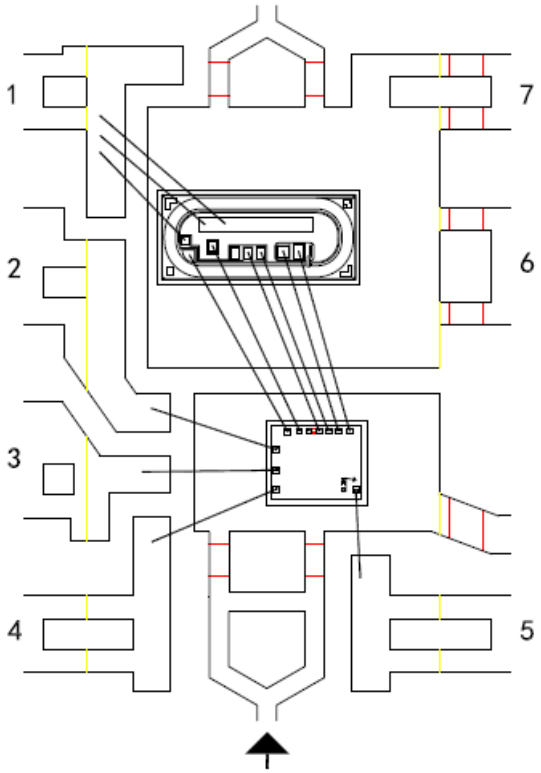
2.2 Pin connection



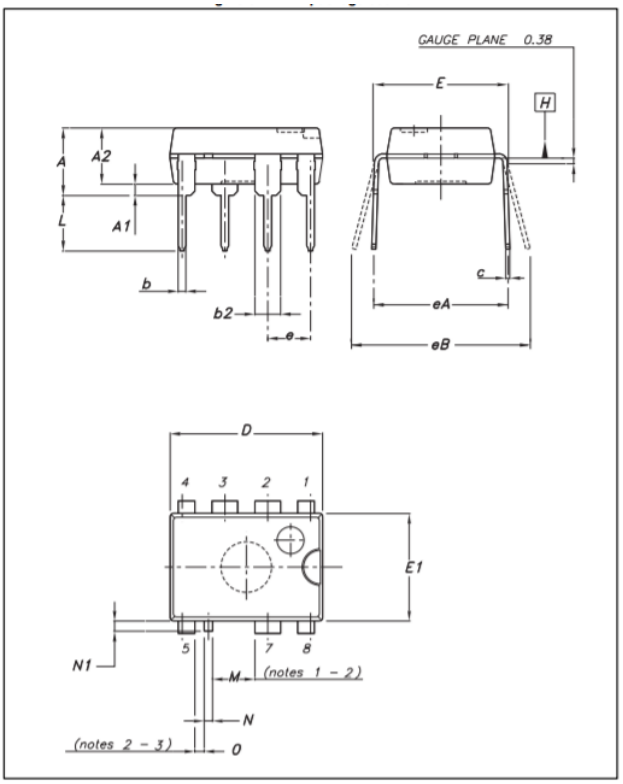
2.3 Block diagram



2.4 Bonding diagram



2.5 Package Outline / Mechanical data



Dim.	mm			Notes
	Min.	Typ.	Max.	
A			5.33	
A1	0.38			
A2	2.92	3.30	4.95	
b	0.36	0.46	0.56	
b2	1.14	1.52	1.78	
c	0.20	0.25	0.36	
D	9.02	9.27	10.16	
E	7.62	7.87	8.26	
E1	6.10	6.35	7.11	
e		2.54		
eA		7.62		
eB			10.92	
L	2.92	3.30	3.81	
M(1)(2)		2.508		6 - 8
N	0.40	0.50	0.60	
N1			0.60	
O(2)(3)		0.548		7 - 8

2.6 Traceability

2.6.1 Wafer fab information

Table 1

Wafer fab information	
UL39	
Wafer fab name / location	CATANIA
Wafer diameter (inches)	8
Die thickness (µm)	375
Silicon process technology	BCD6
Die finishing front side (passivation)	TEOS/SiN/Polymide
Die finishing back side	RAW SILICON SINGLE GRIND
Die area (X,Y) (µm)	1320,1112
Metal levels	3
Bond Pad Material	Ti/AlCu/TiNARC

Table 2

Wafer fab information	
VZ8Q	
Wafer fab name / location	Ang Mo Kio – Singapore
Wafer diameter (inches)	6
Die thickness (µm)	280
Silicon process technology	Supermesh
Die finishing front side (passivation)	SiN (nitride)
Die finishing back side	Ti/Ni/Au
Die area (X,Y) (µm)	2650,1290
Metal levels	1
Bond Pad Material	AlSi

2.6.2 Assembly information

Table 3

Assembly Information	
DIP7	
Assembly plant name	*TFME*
Lead frame finishing (material)	*DIP7LM Cu Ring*
Die attach material	*ABLEBOND 8200T*
Wire bonding material/diameter	*D1.0 AU WIRE*
Molding compound material	*EMG-400-1F (HHCK)*

2.6.3 Reliability information

Table 4

Reliability Information	
Reliability laboratory name / location	Agrate-Cornaredo / Italy (lot 1,2,3) Muar / Malaysia (lot 4,5,6)

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 5

Lot #	Diffusion Lot	Die Revision (Cut)	Raw Line	Package	Note
1	V5840WY9	BG6	RFJG*MV34BG6	DIP7	DA *ABLESTIK 8390S25*
2	V584258M	BE6	FEJG*MV61BE6	DIP7	Equivalent Test Vehicle
3	V5819UU6	AEX	FU(E*MT19AEX	SDIP10	Equivalent Test Vehicle
4	V5017W75	BG6	1UJG*MV34BG6	DIP7	
5	V50121WF	BE6	1UJG*MV61BE6	DIP7	Equivalent Test Vehicle
6	V5009H09	AC6	1UJG*MT13AC6	DIP7	Equivalent Test Vehicle

3.2 Test plan and results summary

Table 6 – ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	VCC=23V TJ=150°C Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	45	135	Lot 1: 0 / 45 Lot 2: 0 / 45 Lot 3: 0 / 45	
HTRB	JESD22 A108	VDRAIN=640V VCC=23V TJ=150°C Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	45	135	Lot 1: 0 / 45 Lot 2: 0 / 45 Lot 3: 0 / 45	

Note: Test method revision reference is the one active at the date of reliability trial execution.

Table 7 – ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
THB	JESD22 A101	VDRAIN=100V VCC=23V Ta=85°C, 85%RH, Duration= 1000hrs ☐ After PC ☒ Testing at Room	2 1	40 25	80 25	Lot 1: 0 / 40 Lot 2: 0 / 40 Lot 3: 0 / 25	
TC	JESD22-A104	Ta= Duration= 500cy ☐ After PC ☒ Testing at Room	3 1	25 77	75 77	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25 Lot 4: 0 / 77 Lot 5: 0 / 77 Lot 6: 0 / 77	
AC	JESD22 A102	P=2.08atm Ta=121°C, Duration = 96hrs ☐ After PC ☒ Testing at Room	3	25	75	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25	
HTSL	JESD22 A103	Ta= 150ºC Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	25	75	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25	

Note: Test method revision reference is the one active at the date of reliability trial execution.

Table 8 – ELECTRICAL VERIFICATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results Fail/S.S.	Comments: (N/A =Not Applicable)
CDM	ANSI/ESDA/JEDEC JS002	CDM=+/-1500V ☒ Testing at Room	3	3	9	Lot 1: 0 / 3 Lot 2: 0 / 3 Lot 3: 0 / 3	

Note: Test method revision reference is the one active at the date of reliability trial execution.

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
AEC-Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits in automotive applications
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
DMS 0061692	Reliability Tests and Criteria for Product Qualification

5 GLOSSARY

List update based on applicable items.

AC	Autoclave
ACBV	AC Blocking Voltage
ASER	Accelerated Soft Error Rate
AST	Adhesion Shear Test
BI	Burn-In
BT3P	Board 3 points Bending Test
BT4P	Board 4 points Bending Test
CA	Constant Acceleration
CDM	Electrostatic Discharge – Charged Device Model
ConA	Construction Analysis
CVS	Constant Voltage Stress
DBT	Dead Bug Test
DPA	Destructive Physical Analysis
DROP	Package drop
DS	Die Shear
DToB	Drop Test on Board
EDR	NVM Program/Erase Endurance & Data Retention Stress Test
ELFR	Early Life Failure Rate
EMC	Electromagnetic Compatibility
EOS	Electrical Overstress characterization
ESeq	Environmental sequence
EV	External Visual
GFF	
GFL	Gross/Fine Leak
GL	Electro-thermally Induced Gate Leakage
GStress	Gate Stress
GUN	Electrostatic Discharge – System Level Test
H3TRB	High Humidity High Temperature Reverse Bias
HAST	Biased HAST (Highly Accelerated Stress Test)
HBM	Electrostatic Discharge – Human Body Model
HER	Hermeticity
HMM	Electrostatic Discharge – Human Metal Model
HTFB	High Temperature Forward Bias
HTGB	High Temperature Gate Bias
HTHHB	High Temperature High Humidity Bias
HTOL	High Temperature Operating Life
HTRB	High Temperature Reverse Bias.
HTSL	High Temperature Storage Life
IOL	Intermittent Operating Life
IWV	Internal Water Vapor
LF	Lead Free
LI	Lead Integrity
LT	Lid Torque
LTOL	Low Temperature Operating Life
LTSL	Low Temperature Storage Life
LU	Latch-Up
MM	Electrostatic Discharge – Machine model

MR	Multiple Reflow
MS	Mechanical Shock
MSeq	Mechanical sequence
MSL	Moisture Sensitivity Level
NVM	Non Volatile Memory
PC	Preconditioning
PD	Physical Dimensions
PTC	Power Temperature Cycling
RS	Repetitive Surge Test
TSH	Resistance to Solder Heat
RTSER	Real-Time Soft Error Rate
SAM	Scanning Acoustic Microscopy
SBP	Solder Ball Pull
SBS	Solder Ball Shear
SC	Short Circuit Characterization
SCCSS	Smartcard – Constant Supply Stress
SCMCMS	Smartcard – MasterCard Mechanical Stress
SCMF	Smartcard – Magnetic Field Stress
SCPOOS	Smartcard – Power Off/On Stress
SCRFC	Smartcard – RF On/Off Cyclic Stress
SCRFS	Smartcard – RF On Static Stress
ScrT	Screw Test
SCSA	Smartcard – Salt Atmosphere
SCUV	Smartcard – UV Test
SCXRAY	Smartcard – XRAY Test
SD	Solderability
SSOP	Steady State Operational
SToB	Shock Test on Board
TC	Temperature Cycling
TCDT	Temperature Cycling Delamination Test
TCHT	Temperature Cycling Hot Test
TCoB	Temperature Cycling on Board
THB	Temperature Humidity Bias
THS	Temperature Humidity Storage
TLP	Electrostatic Discharge – Transmission Line Pulse
TS	Thermal Shocks
TStr	Terminal Strength
Tumb	Tumbler Test
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
VToB	Vibration Test on Board
VFV	Variable Frequency Vibration
WAT	Tin (Sn) Whisker Acceptance Testing
WBI	Wire Bond Integrity
WBP	Wire Bond Pull
WBS	Wire Bond Shear
WBSt	Wire Bond Strength
XRAY	X ray inspection

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Reliability Report
RR001421CO6410

General Information	
Product Line	*MV61 (UP40+VL8Q)*
Product Description	*Off-line Converter*
Package	*DIP7*
Silicon Technology	*BCD6 (UP40)* *Supermesh (VL8Q)*

Traceability	
Diffusion Plant	*Catania* *Ang Mo Kio (Singapore)*
Assembly Plant	*TFME*

Reliability Assessment	
Pass	☒
Fail	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Content description	Date	Author	Function
1.0	Initial Revision	05-Mar-21	P. Teruzzi/G. Capodici	Reliability Engineer

APPROVED BY:

Function	Location	Name
Division Reliability Manager	Italy	A. Paratore
Division Quality Manager	Italy	A. Platini

Table of Contents

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

MV61 is an already qualified device. This report contains the reliability evaluation of MV61 device diffused in Catania/Ang Mo Kio and assembled in Dip7 in TFME, in the overall plan of 8200T Glue and DIP7LM(S-Ag) with Cu Ring lead frame qualification including also other test vehicle.

1.2 Reliability Strategy

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification and are listed in below Test Plan. For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.3 Conclusion

All reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing.

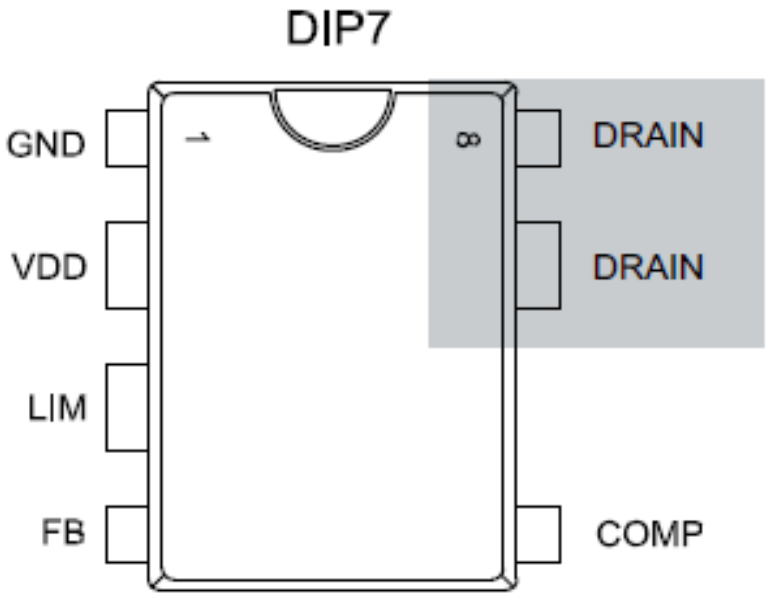
Based on the overall results obtained, MV61 device diffused in Catania/Ang Mo Kio and assembled in Dip7 in TFME, has positively passed reliability evaluation.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

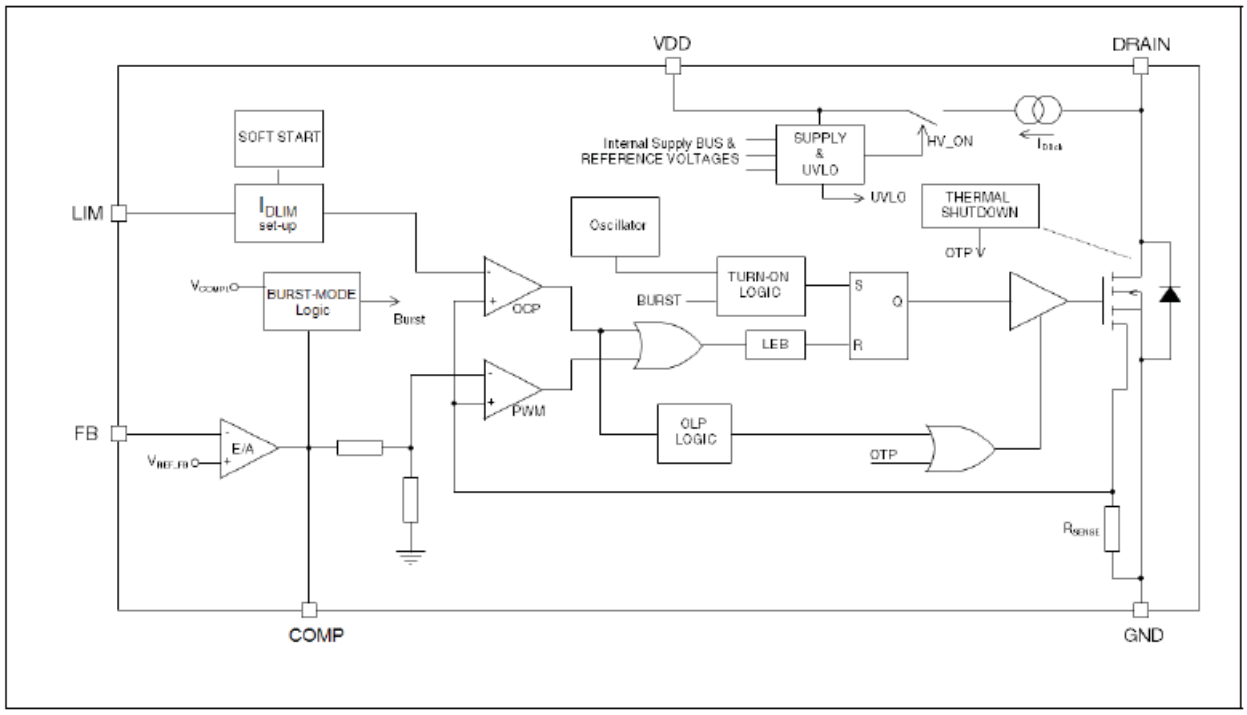
2.1 Generalities

The device is an off-line converter with an 800 V avalanche ruggedness power section, a PWM controller, user defined overcurrent limit, protection against feedback network disconnection, hysteretic thermal protection, soft start up and safe auto restart after any fault condition.

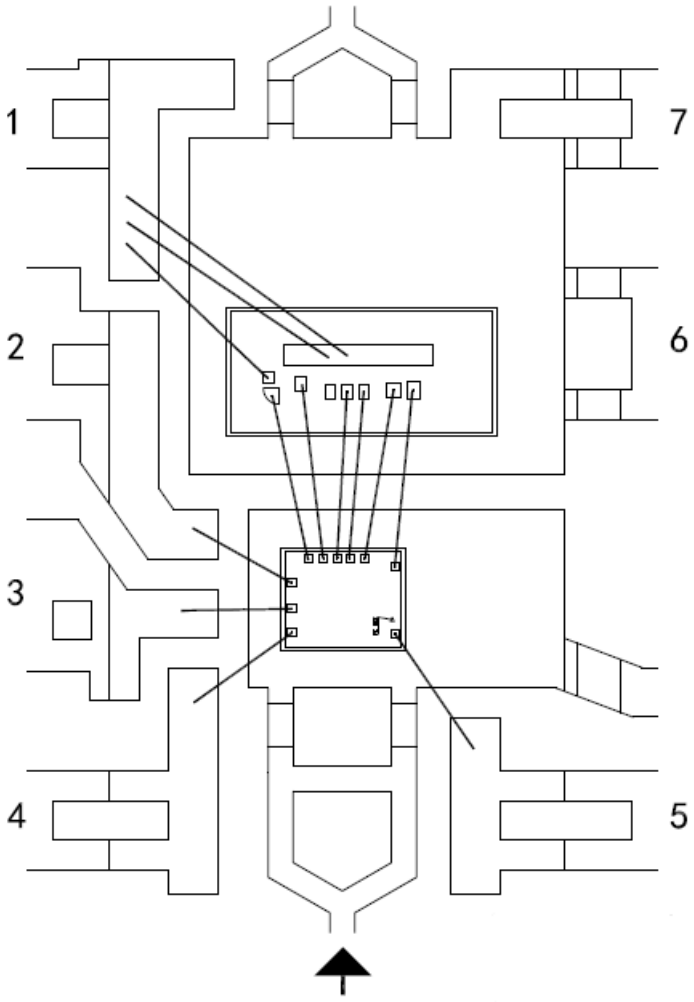
2.2 Pin connection



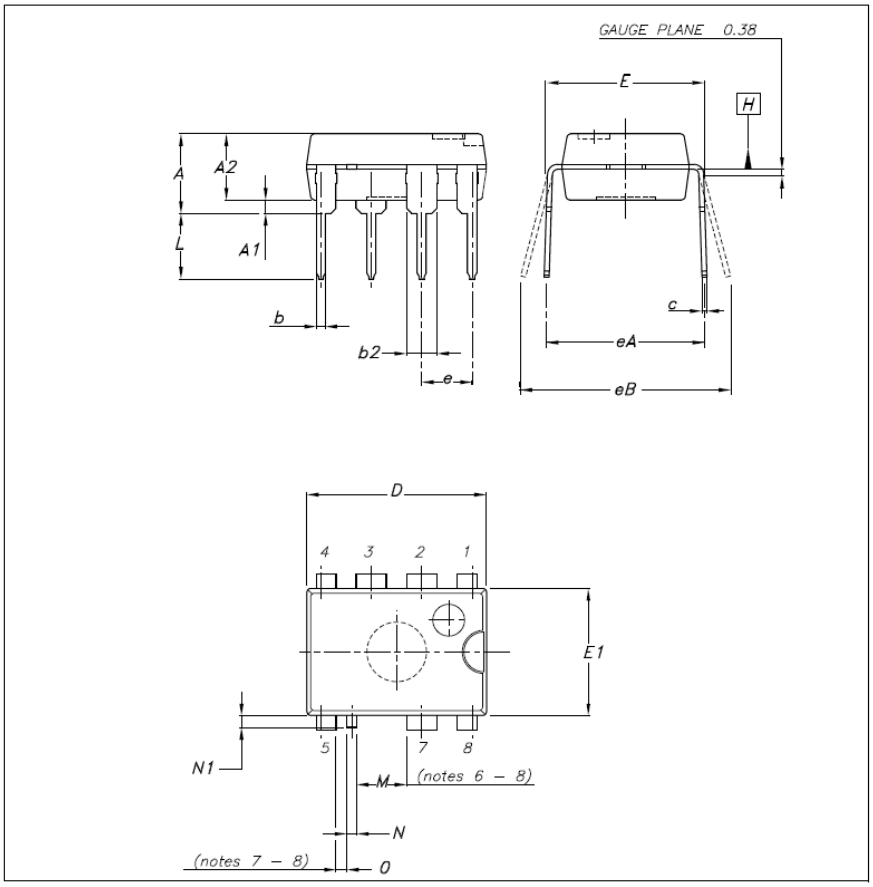
2.3 Block diagram



2.4 Bonding diagram



2.5 Package Outline / Mechanical data



Dim.	mm		
	Typ	Min	Max
A			5,33
A1		0,38	
A2	3,30	2,92	4,95
b	0,46	0,36	0,56
b2	1,52	1,14	1,78
c	0,25	0,20	0,36
D	9,27	9,02	10,16
E	7,87	7,62	8,26
E1	6,35	6,10	7,11
e	2,54		
eA	7,62		
eB			10,92
L	3,30	2,92	3,81
M (6)(8)	2,508		
N	0,50	0,40	0,60
N1			0,60
O (7)(8)	0,548		

2.6 Traceability

2.6.1 Wafer fab information

Table 1

Wafer fab information	
UP40	
Wafer fab name / location	CATANIA
Wafer diameter (inches)	8
Die thickness (µm)	375
Silicon process technology	BCD6
Die finishing front side (passivation)	TEOS/SiN/Polymide
Die finishing back side	RAW SILICON SINGLE GRIND
Die area (X,Y) (µm)	1320,1112
Metal levels	3
Bond Pad Material	Ti/AlCu/TiNARC

Table 2

Wafer fab information	
VL8Q	
Wafer fab name / location	Ang Mo Kio – Singapore
Wafer diameter (inches)	6
Die thickness (µm)	280
Silicon process technology	Supermesh
Die finishing front side (passivation)	SiN (nitride)
Die finishing back side	Ti/Ni/Au
Die area (X,Y) (µm)	2650,1290
Metal levels	1
Bond Pad Material	AlSi

2.6.2 Assembly information

Table 3

Assembly Information	
DIP7	
Assembly plant name	*TFME*
Lead frame finishing (material)	*DIP7LM Cu Ring*
Die attach material	*ABLEBOND 8200T*
Wire bonding material/diameter	*D1.0 AU WIRE*
Molding compound material	*EMG-400-1F (HHCK)*

2.6.3 Reliability information

Table 4

Reliability Information	
Reliability laboratory name / location	Agrate-Cornaredo / Italy (lot 1,2,3) Muar / Malaysia (lot 4,5,6)

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 5

Lot #	Diffusion Lot	Die Revision (Cut)	Raw Line	Package	Note
1	V584258M	BE6	FEJG*MV61BE6	DIP7	DA ABLESTIK 8390S25
2	V5840WY9	BG6	RFJG*MV34BG6	DIP7	Equivalent Test Vehicle
3	V5819UU6	AEX	FU(E*MT19AEX	SDIP10	Equivalent Test Vehicle
4	V50121WF	BE6	1UJG*MV61BE6	DIP7	
5	V5017W75	BG6	1UJG*MV34BG6	DIP7	Equivalent Test Vehicle
6	V5009H09	AC6	1UJG*MT13AC6	DIP7	Equivalent Test Vehicle

3.2 Test plan and results summary

Table 6 – ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	VCC=23V TJ=150°C Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	45	135	Lot 1: 0 / 45 Lot 2: 0 / 45 Lot 3: 0 / 45	
HTRB	JESD22 A108	VDRAIN=640V VCC=23V TJ=150°C Duration= 1000hrs ☐ After PC ☒ Testing at Room	2	45	135	Lot 1: 0 / 45 Lot 2: 0 / 45 Lot 3: 0 / 45	

Note: Test method revision reference is the one active at the date of reliability trial execution.

Table 7 – ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
THB	JESD22 A101	VDRAIN=100V VCC=23V Ta=85°C, 85%RH, Duration= 1000hrs ☐ After PC ☒ Testing at Room	2 1	40 25	80 25	Lot 1: 0 / 40 Lot 2: 0 / 40 Lot 3: 0 / 25	
TC	JESD22-A104	Ta= Duration= 500cy ☐ After PC ☒ Testing at Room	3 1	25 77	75 77	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25 Lot 4: 0 / 77 Lot 5: 0 / 77 Lot 6: 0 / 77	
AC	JESD22 A102	P=2.08atm Ta=121°C, Duration = 96hrs ☐ After PC ☒ Testing at Room	3	25	75	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25	
HTSL	JESD22 A103	Ta= 150ºC Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	25	75	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25	

Note: Test method revision reference is the one active at the date of reliability trial execution.

Table 8 – ELECTRICAL VERIFICATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results Fail/S.S.	Comments: (N/A =Not Applicable)
CDM	ANSI/ESDA/JEDEC JS002	CDM=+/-1500V ☒ Testing at Room	3	3	9	Lot 1 :0 / 3 Lot 2 :0 / 3 Lot 3 :0 / 3	

Note: Test method revision reference is the one active at the date of reliability trial execution.

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
AEC-Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits in automotive applications
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
DMS 0061692	Reliability Tests and Criteria for Product Qualification

5 GLOSSARY

List update based on applicable items.

AC	Autoclave
ACBV	AC Blocking Voltage
ASER	Accelerated Soft Error Rate
AST	Adhesion Shear Test
BI	Burn-In
BT3P	Board 3 points Bending Test
BT4P	Board 4 points Bending Test
CA	Constant Acceleration
CDM	Electrostatic Discharge – Charged Device Model
ConA	Construction Analysis
CVS	Constant Voltage Stress
DBT	Dead Bug Test
DPA	Destructive Physical Analysis
DROP	Package drop
DS	Die Shear
DToB	Drop Test on Board
EDR	NVM Program/Erase Endurance & Data Retention Stress Test
ELFR	Early Life Failure Rate
EMC	Electromagnetic Compatibility
EOS	Electrical Overstress characterization
ESeq	Environmental sequence
EV	External Visual
GFF	
GFL	Gross/Fine Leak
GL	Electro-thermally Induced Gate Leakage
GStress	Gate Stress
GUN	Electrostatic Discharge – System Level Test
H3TRB	High Humidity High Temperature Reverse Bias
HAST	Biased HAST (Highly Accelerated Stress Test)
HBM	Electrostatic Discharge – Human Body Model
HER	Hermeticity
HMM	Electrostatic Discharge – Human Metal Model
HTFB	High Temperature Forward Bias
HTGB	High Temperature Gate Bias
HTHHB	High Temperature High Humidity Bias
HTOL	High Temperature Operating Life
HTRB	High Temperature Reverse Bias.
HTSL	High Temperature Storage Life
IOL	Intermittent Operating Life
IWV	Internal Water Vapor
LF	Lead Free
LI	Lead Integrity
LT	Lid Torque
LTOL	Low Temperature Operating Life
LTSL	Low Temperature Storage Life
LU	Latch-Up
MM	Electrostatic Discharge – Machine model

MR	Multiple Reflow
MS	Mechanical Shock
MSeq	Mechanical sequence
MSL	Moisture Sensitivity Level
NVM	Non Volatile Memory
PC	Preconditioning
PD	Physical Dimensions
PTC	Power Temperature Cycling
RS	Repetitive Surge Test
TSH	Resistance to Solder Heat
RTSER	Real-Time Soft Error Rate
SAM	Scanning Acoustic Microscopy
SBP	Solder Ball Pull
SBS	Solder Ball Shear
SC	Short Circuit Characterization
SCCSS	Smartcard – Constant Supply Stress
SCMCMS	Smartcard – MasterCard Mechanical Stress
SCMF	Smartcard – Magnetic Field Stress
SCPOOS	Smartcard – Power Off/On Stress
SCRFC	Smartcard – RF On/Off Cyclic Stress
SCRFS	Smartcard – RF On Static Stress
ScrT	Screw Test
SCSA	Smartcard – Salt Atmosphere
SCUV	Smartcard – UV Test
SCXRAY	Smartcard – XRAY Test
SD	Solderability
SSOP	Steady State Operational
SToB	Shock Test on Board
TC	Temperature Cycling
TCDT	Temperature Cycling Delamination Test
TCHT	Temperature Cycling Hot Test
TCoB	Temperature Cycling on Board
THB	Temperature Humidity Bias
THS	Temperature Humidity Storage
TLP	Electrostatic Discharge – Transmission Line Pulse
TS	Thermal Shocks
TStr	Terminal Strength
Tumb	Tumbler Test
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
VToB	Vibration Test on Board
VFV	Variable Frequency Vibration
WAT	Tin (Sn) Whisker Acceptance Testing
WBI	Wire Bond Integrity
WBP	Wire Bond Pull
WBS	Wire Bond Shear
WBSt	Wire Bond Strength
XRAY	X ray inspection

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Reliability Report
RR007221CO6410

General Information	
Product Line	*VNB7*
Product Description	*Low power OFF-line SMPS primary switcher*
Package	*DIP8*
Silicon Technology	*VIPower M03*

Traceability	
Diffusion Plant	*Ang Mo Kio (Singapore)*
Assembly Plant	*TFME – FUJITSU*

Reliability Assessment	
Pass	☒
Fail	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Content description	Date	Author	Function
1.0	Initial Revision	22-Nov-21	P. Teruzzi/G. Capodici	Reliability Engineer

APPROVED BY:

Function	Location	Name
Division Reliability Manager	Italy	A. Paratore
Division Quality Manager	Italy	A. Platini

Table of Contents

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

VNB7 is an already qualified device. This report contains the reliability evaluation of VNB7 device diffused in Ang Mo Kio and assembled in DIP8 in TFME, in the overall plan of 8200T Glue and DIP8 lead frame qualification including also other test vehicle.

1.2 Reliability Strategy

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification and are listed in below Test Plan. For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.3 Conclusion

All reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing.

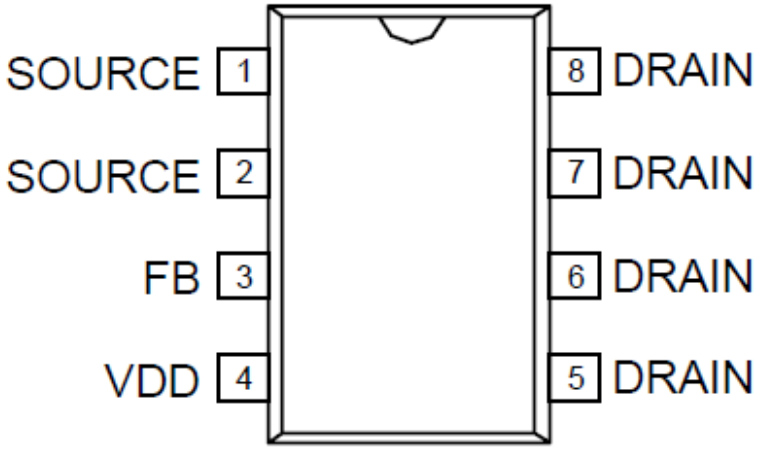
Based on the overall results obtained, VNB7 device diffused in Ang Mo Kio and assembled in DIP8 in TFME-FUJITSU, has positively passed reliability evaluation.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

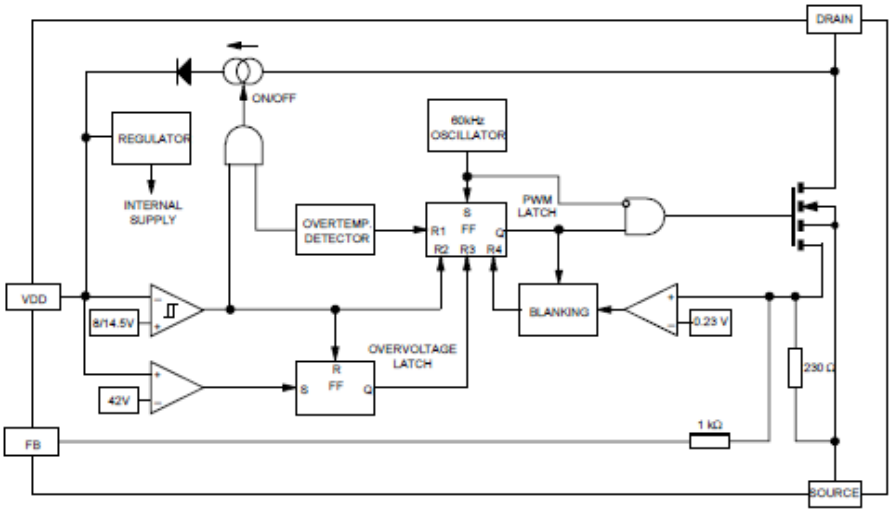
The VIPer22A-E combines a dedicated current mode PWM controller with a high voltage power MOSFET on the same silicon chip. Typical applications cover off line power supplies for battery charger adapters, standby power supplies for TV or monitors, auxiliary supplies for motor control, etc.

2.2 Pin connection

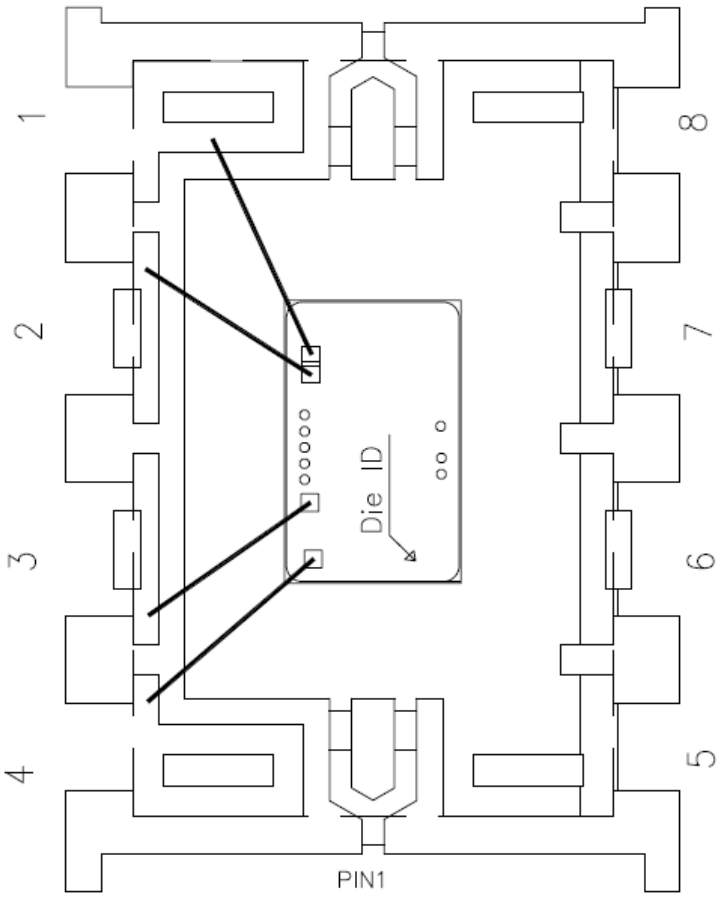


DIP-8

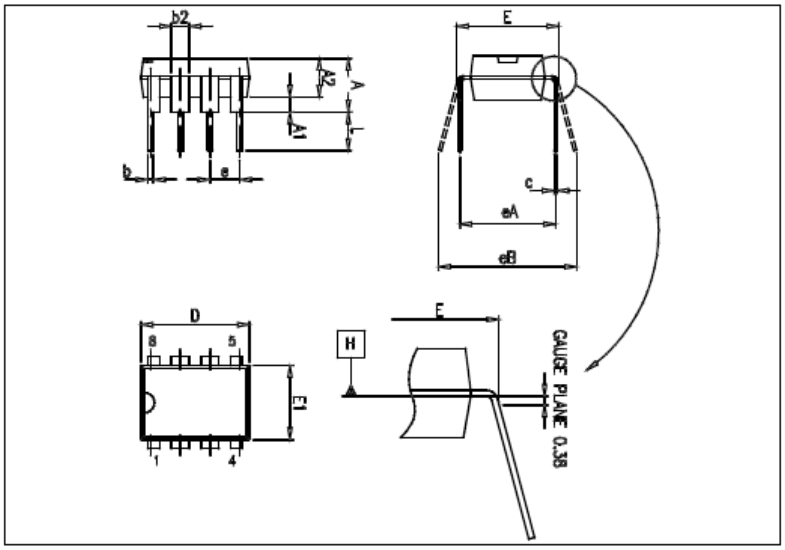
2.3 Block diagram



2.4 Bonding diagram



2.5 Package Outline / Mechanical data



Dim.	Databook (mm.)		
	Min.	Nom.	Max.
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.26
E1	6.10	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81
Package Weight	Gr. 470		

2.6 Traceability

2.6.1 Wafer fab information

Table 1

Wafer fab information	
VNB7	
Wafer fab name / location	Ang Mo Kio
Wafer diameter (inches)	6
Die thickness (µm)	280
Silicon process technology	VIPower M03
Die finishing front side (passivation)	SiN (nitride)
Die finishing back side	Ti-Ni-Au
Die area (X,Y) (µm)	3250,2070
Metal levels	1
Bond Pad Material	AlSi

2.6.2 Assembly information

Table 3

Assembly Information	
DIP8	
Assembly plant name	*TFME*
Lead frame finishing (material)	*DIP8 Cu Ring*
Die attach material	*ABLEBOND 8200T*
Wire bonding material/diameter	*Au 1.3 mils*
Molding compound material	*MG46FAM*

2.6.3 Reliability information

Table 4

Reliability Information	
Reliability laboratory name / location	Agrate-Cornaredo / Italy (lot 1,2,3,7) Muar / Malaysia (lot 4,5,6.8)

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 5

Lot #	Diffusion Lot	Die Revision (Cut)	Raw Line	Package	Note
1	V584258M	BE6	FEJG*MV61BE6	DIP7	Equivalent Test vehicle
2	V5840WY9	BG6	RFJG*MV34BG6	DIP7	Equivalent Test vehicle
3	V5819UU6	AEX	FU(E*MT19AEX	SDIP10	Equivalent Test vehicle
4	V5009H09	AC6	1UJG*MT13AC6	DIP7	Equivalent Test vehicle
5	V50121WF	BE6	1UJG*MV61BE6	DIP7	Equivalent Test vehicle
6	V5017W75	BG6	1UJG*MV34BG6	DIP7	Equivalent Test vehicle
7	KYA938	AA5	A5(E*MT13AA5	DIP7	Equivalent Test vehicle
8	9996660CK	WCA	9F8W*VNB7WCA	DIP8	

3.2 Test plan and results summary

Table 6 – ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	VCC=23V TJ=150°C Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	45	135	Lot 1: 0 / 45 Lot 2: 0 / 45 Lot 3: 0 / 45	
HTRB	JESD22 A108	VDRAIN=640V VCC=23V TJ=150°C Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	45	135	Lot 1: 0 / 45 Lot 2: 0 / 45 Lot 3: 0 / 45	

Note: Test method revision reference is the one active at the date of reliability trial execution.

Table 7 – ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
THB	JESD22 A101	VDRAIN=100V VCC=23V Ta=85°C, 85%RH, Duration= 1000hrs ☐ After PC ☒ Testing at Room	2 1	40 25	80 25	Lot 1: 0 / 40 Lot 2: 0 / 40 Lot 3: 0 / 25	
TC	JESD22-A104	Ta= Duration= 500cy ☐ After PC ☒ Testing at Room	3 3 1	25 77 77	75 231 77	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25 Lot 4: 0 / 77 Lot 5: 0 / 77 Lot 6: 0 / 77 Lot8: 0 / 77	
AC	JESD22 A102	P=2.08atm Ta=121°C, Duration = 96hrs ☐ After PC ☒ Testing at Room	3	25	75	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25	
HTSL	JESD22 A103	Ta= 150ºC Duration= 1000hrs ☐ After PC ☒ Testing at Room	3	25	75	Lot 1: 0 / 25 Lot 2: 0 / 25 Lot 3: 0 / 25	

Note: Test method revision reference is the one active at the date of reliability trial execution.

Table 8 – ELECTRICAL VERIFICATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results Fail/S.S.	Comments: (N/A =Not Applicable)
CDM	ANSI/ESD STM 5.3.1-2009	CDM=+/-1500V ☒ Testing at Room	1	3	3	Lot 7 :0 / 3	
MM	EIA/JESD22-A115	MM=+/-200V ☒ Testing at Room	1	3	3	Lot 7 :0 / 3	
HBM	ANSI/ESDA/JEDEC JS001-2014	HBM=+/-4000V ☒ Testing at Room	1	3	3	Lot 7 :0 / 3	
LU	JESD78	Current Injection Class II - Level B (+/- 100mA) Overvoltage Class II - Level B (1,5 x Vmax) ☐ Testing at Room	1	6	6	Lot 7 :0 / 6	

Note: Test method revision reference is the one active at the date of reliability trial execution.

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
AEC-Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits in automotive applications
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
DMS 0061692	Reliability Tests and Criteria for Product Qualification

5 GLOSSARY

List update based on applicable items.

AC	Autoclave
ACBV	AC Blocking Voltage
ASER	Accelerated Soft Error Rate
AST	Adhesion Shear Test
BI	Burn-In
BT3P	Board 3 points Bending Test
BT4P	Board 4 points Bending Test
CA	Constant Acceleration
CDM	Electrostatic Discharge – Charged Device Model
ConA	Construction Analysis
CVS	Constant Voltage Stress
DBT	Dead Bug Test
DPA	Destructive Physical Analysis
DROP	Package drop
DS	Die Shear
DToB	Drop Test on Board
EDR	NVM Program/Erase Endurance & Data Retention Stress Test
ELFR	Early Life Failure Rate
EMC	Electromagnetic Compatibility
EOS	Electrical Overstress characterization
ESeq	Environmental sequence
EV	External Visual
GFF	
GFL	Gross/Fine Leak
GL	Electro-thermally Induced Gate Leakage
GStress	Gate Stress
GUN	Electrostatic Discharge – System Level Test
H3TRB	High Humidity High Temperature Reverse Bias
HAST	Biased HAST (Highly Accelerated Stress Test)
HBM	Electrostatic Discharge – Human Body Model
HER	Hermeticity
HMM	Electrostatic Discharge – Human Metal Model
HTFB	High Temperature Forward Bias
HTGB	High Temperature Gate Bias
HTHHB	High Temperature High Humidity Bias
HTOL	High Temperature Operating Life
HTRB	High Temperature Reverse Bias.
HTSL	High Temperature Storage Life
IOL	Intermittent Operating Life
IWV	Internal Water Vapor
LF	Lead Free
LI	Lead Integrity
LT	Lid Torque
LTOL	Low Temperature Operating Life
LTSL	Low Temperature Storage Life
LU	Latch-Up
MM	Electrostatic Discharge – Machine model

MR	Multiple Reflow
MS	Mechanical Shock
MSeq	Mechanical sequence
MSL	Moisture Sensitivity Level
NVM	Non Volatile Memory
PC	Preconditioning
PD	Physical Dimensions
PTC	Power Temperature Cycling
RS	Repetitive Surge Test
TSH	Resistance to Solder Heat
RTSER	Real-Time Soft Error Rate
SAM	Scanning Acoustic Microscopy
SBP	Solder Ball Pull
SBS	Solder Ball Shear
SC	Short Circuit Characterization
SCCSS	Smartcard – Constant Supply Stress
SCMCMS	Smartcard – MasterCard Mechanical Stress
SCMF	Smartcard – Magnetic Field Stress
SCPOOS	Smartcard – Power Off/On Stress
SCRFC	Smartcard – RF On/Off Cyclic Stress
SCRFS	Smartcard – RF On Static Stress
ScrT	Screw Test
SCSA	Smartcard – Salt Atmosphere
SCUV	Smartcard – UV Test
SCXRAY	Smartcard – XRAY Test
SD	Solderability
SSOP	Steady State Operational
SToB	Shock Test on Board
TC	Temperature Cycling
TCDT	Temperature Cycling Delamination Test
TCHT	Temperature Cycling Hot Test
TCoB	Temperature Cycling on Board
THB	Temperature Humidity Bias
THS	Temperature Humidity Storage
TLP	Electrostatic Discharge – Transmission Line Pulse
TS	Thermal Shocks
TStr	Terminal Strength
Tumb	Tumbler Test
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
VToB	Vibration Test on Board
VFV	Variable Frequency Vibration
WAT	Tin (Sn) Whisker Acceptance Testing
WBI	Wire Bond Integrity
WBP	Wire Bond Pull
WBS	Wire Bond Shear
WBSt	Wire Bond Strength
XRAY	X ray inspection

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